International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Vol. 4, No. 3, July 2015

Research Paper

DESIGN AND IMPLEMENTATION OF TRACKING RECEIVER REMOTE TERMINAL FPGA CARD FOR SAT-4

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SAT-4 is an advanced communication satellite with multi spot beam antenna. An on-board RF tracking system is required to accurately point the on-board antenna to ground. This on-board tracking system will collect the beacon carriers transmitted by uplink ground beacon terminals, which are processed and sent to the receiver and points the antenna to the desired position. The on-board RF Tracking system consists of Tracking Receiver Remote Terminal (TRRT) Interface unit which collects error and control signals from Receiver/Transmitter control unit. This TRRT interface unit consisting of FPGA card collects the data from PROM and also the error and control signals from Receiver/Transmitter control unit are stored in SRAM. The summit device collects the stored data from SRAM and processes the signals and corrects it. These corrected signals are given to altitude orbit control system to drive the antenna in the required direction.The MIL-1553 interface, which provides galvanic isolation, is used for the AOCS and Tracking Rx interaction.

Keywords: SAT-4, FPGA, TRRT, WDT, FSM, RF, AOCS, PROM

INTRODUCTION

The SAT-4 satellite will have four Ku band reflectors which are required to be tracked using a single tracking receiver in sequence to reduce costly hardware and mass. The communication cum tracking feed from each reflector provides a sum and error output. The sum output is processed by sum chain and error output is processed by error chain. As sum output contains communication signal along with beacon signal, both are processed by the common hardware till they are divided at hybrid. The sum and error signals from each reflector are selected for processing using sum and error chain RF switch. The selected signals are processed by down converters and tracking receiver to generate DC signals proportional to pointing error in AZ and EL

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directions. The AOCS reads these DC error signals along with Lock-On Status signal and provides the appropriate signals to APM in order to move the selected antenna towards null. The AOCS selects one of the four antennae by sending appropriate commands to sum and error chain RF switches. This project discusses the Design and Implementation of Tracking Receiver Remote Terminal card and also confines itself to discussion of the FPGA Design of Tacking Receiver Remote Terminal Card.

DESIGN IMPLEMENTATION

Figure 1: Functional Blocks of TRRT FPGA

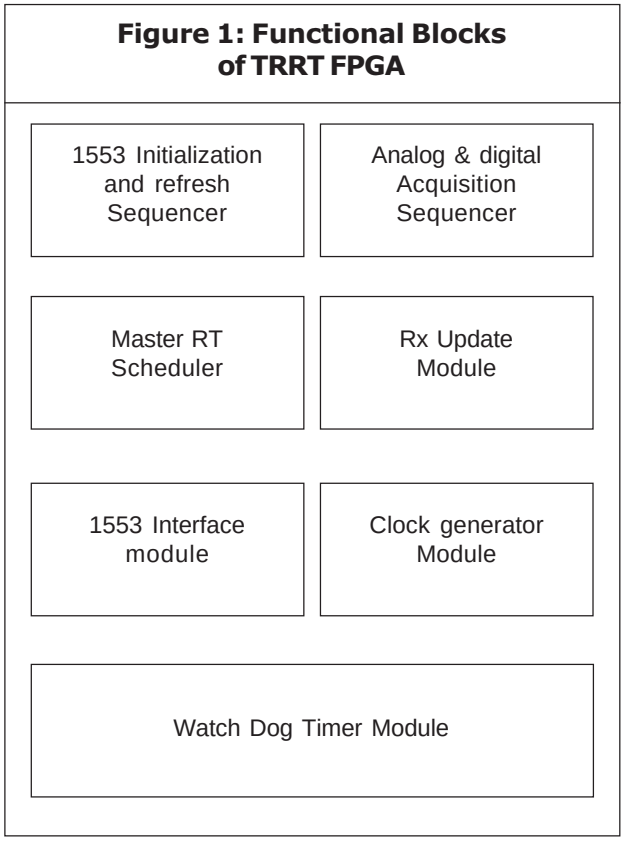


Figure 1 shows the functional blocks of TRRT FPGA card. The FPGA provides the following functions 1553 summit device registers and memory initialization from PROM on POR+Reset Cmd+WDT pulse.Analog sequencer to acquire four analog inputs plus four spare and store the same in independent latches. Store the digital inputs (SILs) in independent latch at the start of every analog acquisition sequence. Time taken for reading each channel is 600us and for all the channels is 4.8ms. the acquired data is transferred to 1553 RAM on receiving data ready from BC.Arbitration logic to access 1553 RAM either by summit device or by the sequencer logic in FPGA.Access for all the 1553 Tx transfers is indicated with an RT access word (data ready) from BC. When the LSB goes from low to high, the Tx data is updated in the FPGA for Tx transfers. As per analysis, BC can read the same after ~1.1ms after setting the data ready signal. Periodical refreshing of 1553 memory initialization (i.e., read a location from PROM and write back the corrected data) is done if refresh logic is enabled. Two location of 1553 memory are refreshed every 40ms.Watch dog timer is provided in case of continuous data ready absence for 3min. It will reinitialize the summit register and 1553 RAM descriptor table from PROM. WDT occurred status and WDT enable/disable status is sent to 1553 memory along the digital input data.Dataready location is read by main scheduler every 1ms; if data ready location is '1' Tx data is updated in 1553 RAM. Data ready is then reset. Main scheduler waits for 8ms to ensure that 1553 shared RAM is not accessed by FPGA.1553 telecommand is provided for internal logic: refresh logic enable/ disable and WDT enable/disable.

Outputs from FPGA: Phase control word received from AOCE through 1553 is latched and output as 12-bit parallel data.Two sets of 2-bits to select one of the 4 antennae. One set

for the antenna switchmatrix-M and the other for switch matrix-R.

1553 Initialization and Refresh Sequencer

This logic is used to initially configure the UTMC chip as RT and load the configuration registers and the descriptor table. This module uses two flags, one for initialization (init_flag_s) high on PoR and the refresh_flag_s asserted by main scheduler. The initialization and refresh functions are shown in Tables 2.1 and 2.2 shows the decoding of control signals read from PROM.

Table 2.1: Status Table for Register and RAM Access

Reg_access_s(1:0)	Init_RAM_access_s(1:0)	Description
01(Default state)	01(Default state)	Memory and register are disable and are in read state
11	01	Register read
10	01	Register write
01	11	Memory read
01	10	Memory write

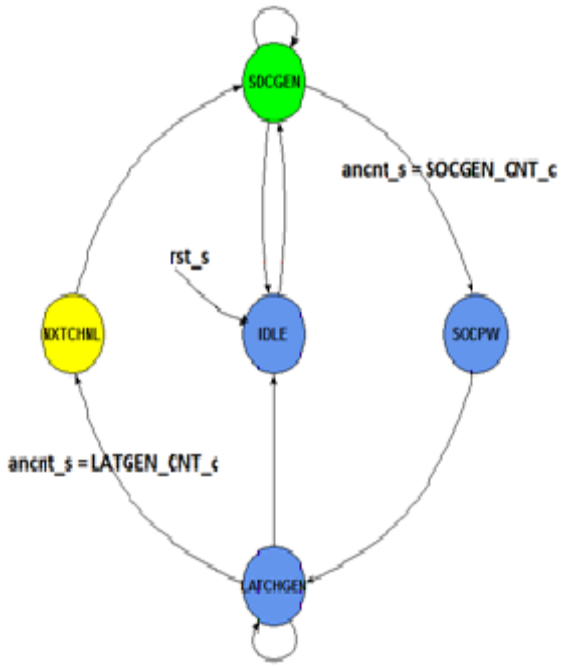
Table 2.2: Decoding of Control Signals Read from PROM

PROM Register bit	Signal name	Description
Prom_rd_data_s(0)(12)	Eofinint_s	End of initialization
Prom_rd_data_s(0)(13)	Init_memregn_s	'0'=Summit register access '1'=1553 SRAM access
Prom_rd_data_s(0)(14)	Init_rdwrn_s	'0'=Write access '1'=Read access
Prom_rd_data_s(0)(15)	NOP_s	No operation

Analog and Digital Data acquisition Sequencer

Analog sequencer module is used to sequence the acquisition of analog and digital inputs. This module is enabled by rt_scheduler with an_seq_endissts_s signal. The FSM is shown in Figure 3.1.

Figure 3.1: FSM of Analog and Digital Data Acquisition Sequencer



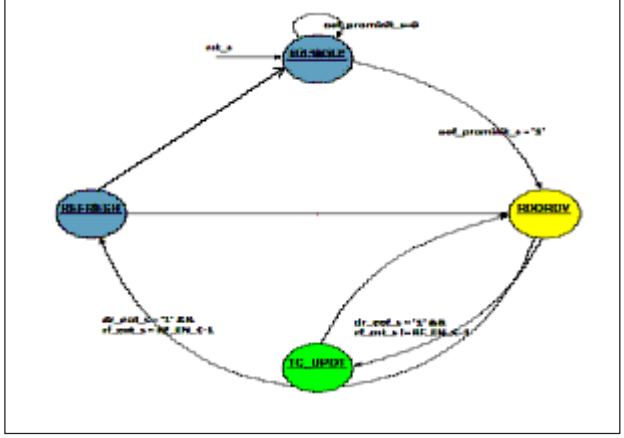
MASTER RT SCHEDULER

This is the main scheduler which enables and disables the other schedulers. This scheduler is initiated after end of initialization of summit registers and 1553 RAM descriptor table. Master scheduler uses SubSeqFlag_s to generate flags for data ready, TC and Refresh scheduler.

Master RT scheduler consists of two sub blocks they are 1.Data ready scheduler used to schedule the ready data 2. Telecommand update scheduler updates the commands.

Figure 4.1 shows the FSM of Master RT scheduler. This module schedules the states in a sequential manner by asserting the corresponding flags.

Figure 4.1 : FSM of Master RT Scheduler



MASIDLE: This is the initial state after PoR Master Scheduler remains in this state until end of initiation indicated by eof_prominit_s.

RDDRDY: Data ready memory location is ready by assigningSubSeqFlag_s= DRDY_FLAG_C. data ready decoding is done in data ready scheduler which generates dr_eof_s to indicate end of the activity. The master scheduler will go to next state only when dr_eof_s is high. After detecting dr_eof_s high and rf_cnt_s=RF_EN_C-1 moved to REFRESH state else moved to TC_UPDT state.

TC_UPDT: Telecommand reading is initiated by assigning SubSeqFlag_s=TC_C. In next cycle rt_sch is moved to RDDRDY.

REFRESH: Refreshing of two RAM locations is performed is read by assigning SubSeqFlag_s=REFRESH_FLAG_C. In the next clock cycle of rt_sch moved to RDDRDY state.

Clock Generator Module

This module generates the clock frequencies of, 1us, 1ms, 8ms, 500us, 83ns and 26us with block diagram shown in Figure 5.1.

Figure 5.1: Clock generator module

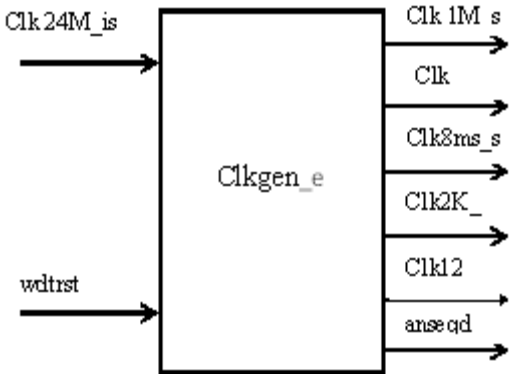


Table 5.1: Frequency Used by Each Module

Sl No	Module	Clock frequency
1	Main scheduler	2KHz
2	Rt_init	1MHz
3	Data ready read and Tx update module	1MHz
4	Analog and digital acquisition sequencer	38KHz(26us)
5	Refresh module	1MHz
6	TC update module	1MHz
7	1553 interface	12 MHz and 24 MHz
8	WDT	125Hz

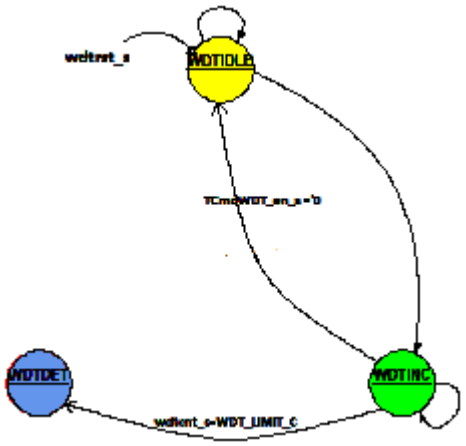
Clock generated by the Clkgen module are used by different modules given in Table 5.1.

Watchdog Timer Module

This module generates the wdt_s of 50ms pulse width if drdy_pulse is not received from AOCE continuous for 3minutes. Block diagram and FSM for WDT is shown in Figure 6.1 and Figure 6.2. WDT reset wdtrst_s is generated by logical ORing of por_is and CmdRst_is. Wdt_occrdsts_s and wdt_endis_s status signals are stored in 1553 RAM in 4^{th} and 5^{th} bit of Tx SA1 W0 at address location 0x0400 with digital acquired data when data ready bit is received from AOCE. Wdt_occrdsts_s status is cleared by telecommand.

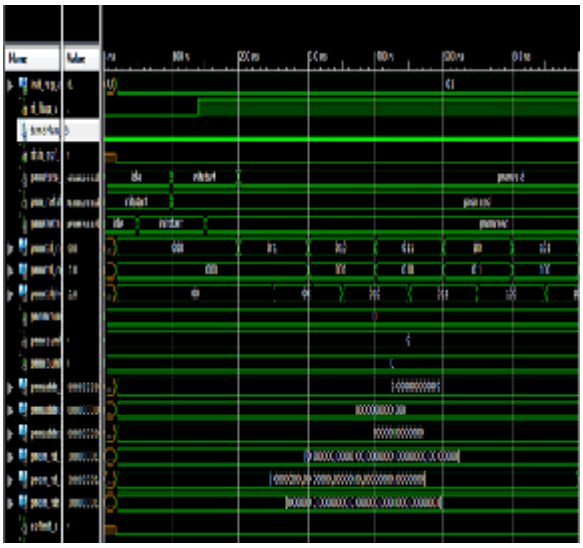
Figure 6.1: Block Diagram of WDT

Figure 6.2: FSM of WDT

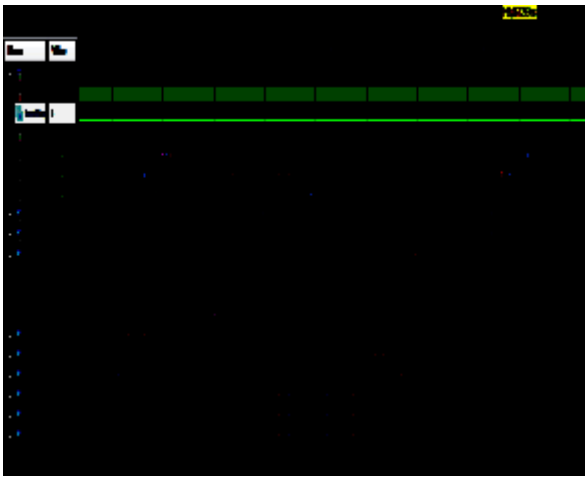


RESULTS

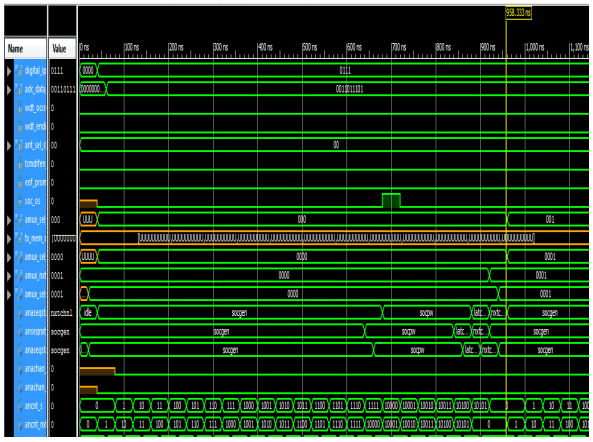
Output of 1553 Initialization Sequencer



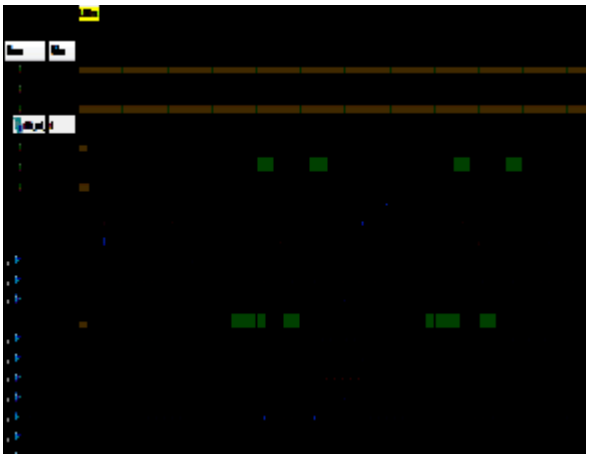
Output of 1553 Refresh Sequencer



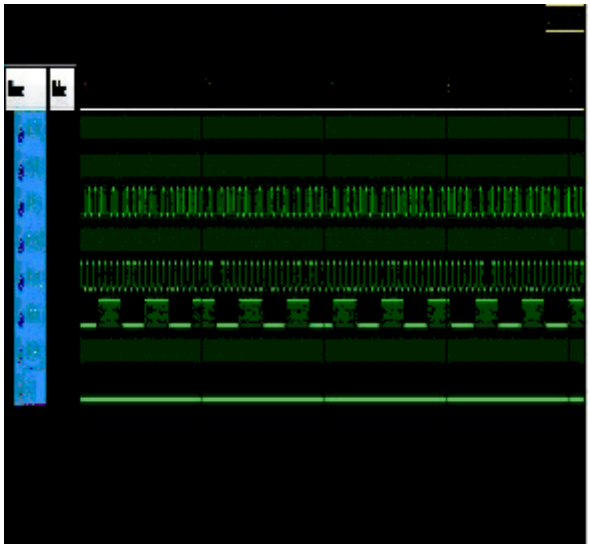
Output of Analog and Digital Data Acquisition Sequencer



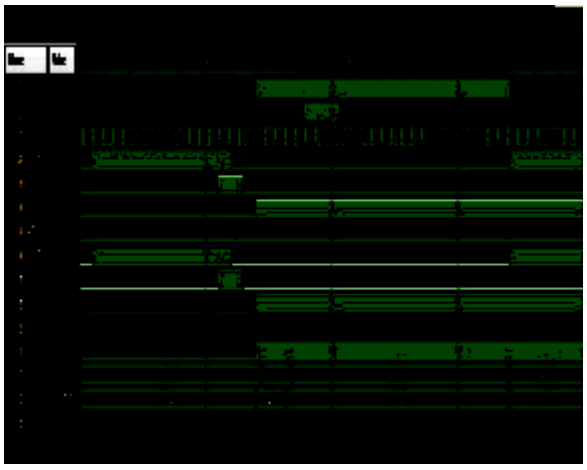
Output of Master RT Scheduler



Output of Clock Generator Module



Output of Watch Dog Timer



CONCLUSION

The objective to design the different blocks of FPGA card which are 1553 Initialization and refresh sequencer, Analog and Digital acquisition sequencer, Master RT Scheduler, 1553 Interface Module, Clock Generator module and Watchdog Timer module is achieved successfully during the course of this project and the results are obtained satisfactorily well ahead of the timeline.

Analog and Digital acquisition sequencer is developed to sequence the acquisition of Analog and Digital inputs. 1553 Initialization and refresh sequencer is developed to initialize and refresh the SRAM. Master RT Scheduler is developed to enable and disable the other schedulers of the FPGA card. 1553 Interface Module is developed for interfacing purpose with the summit device and SRAM. Various clock frequencies are generated for the different blocks of FPGA by the clock generator module. Watchdog timer module is developed to generate the watchdog timer for resetting of the system.

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