# A Study of High-Speed Hamming Distance Detection Circuit Utilizing a Neuron CMOS Inverter

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*Abstract*—**This study tackles the challenge of optimizing associative memory for efficient data retrieval from large databases, crucial in real-time processing. The authors specifically address the issue of increased detection time in the minimum Hamming distance search associative memory, particularly as the number of data bits grows. This memory system utilizes Hamming distance as a key metric to identify the most similar reference data. Our contribution is the development of a new Hamming distance detection circuit employing neuron Complementary Metal Oxide Semiconductor (CMOS) inverters. This proposed circuit significantly outperforms existing models in terms of operational speed. The effectiveness and improved performance of the circuit are validated through simulations using HSPICE, a type of Simulation Program with Integrated Circuit Emphasis (SPICE) demonstrating its potential for more efficient real-time data retrieval applications.**

*Index Terms*—**associative memory, hamming distance, high-speed**

## I. INTRODUCTION

Technologies for high-speed retrieval of the most similar data from data stored in a database, such as face recognition, DNA pattern matching, and image compression, are being used in all kinds of situations [1–3]. Recently, with the proliferation of IoT, the amount of information has increased rapidly, and stream data processing, which processes large amounts of data in real-time, has attracted attention. However, when similarity search processing is performed on a computer, data is called up and compared sequentially, so the search time becomes very large as the number of data to be compared increases. Deep learning is currently being actively researched as a method to improve detection and processing time, including in medical and various other

applications [4–6]. However, this method requires a large amount of data and time for training and is not easy to prepare in advance.

To solve these problems, associative memory, one type of functional memory, has been actively studied [7–12]. Associative memory is a memory that, in addition to the usual memory functions, can perform fast search operations by searching the most similar data to the input data in the database in parallel for comparison. Similarity indices include Hamming distance, Manhattan distance, and Euclidean distance [13, 14]. Hamming distance is used for fingerprint recognition and character recognition, while Manhattan distance and Euclidean distance are used for color image recognition, etc.

Humans are good at association and recognition, and given a fragment of information, they can instantly associate what it is from their vast memory. The authors focused on a neuron Complementary Metal Oxide Semiconductor (CMOS) inverter, which has properties similar to those of neurons in the brain [15]. The neuron CMOS inverter has been studied for application to A/D converters and a variety of other circuits since complex operations can be achieved with a simple circuit configuration [16–19]. Therefore, the authors wondered whether this device could be used to realize a high-speed associative memory with a simple configuration. In a minimum Hamming distance search associative memory that retrieves the most similar data using the Hamming distance as an index, the Hamming distance detection circuit that detects the Hamming distance between two data is a very important functional circuit. The authors' research group has proposed a Hamming distance detection circuit by utilizing a neuron CMOS inverter [20–22]. Conventional circuits detect the Hamming distance by converting the Hamming distance into the time it takes for the output signal to change. Therefore, this circuit has the problem that the detection time increases with each increase in the number of data bits.

To solve this problem, this paper proposes a new Hamming distance detection circuit based on neuron CMOS inverters. The proposed circuit can suppress the increase in time with increasing Hamming distance by varying the capacitance between the input terminal and the floating gate of the neuron CMOS inverter. The operation of this circuit was also verified using HSPICE, a circuit simulator.

## II. CIRCUIT CONFIGURATION

When $A = (a_1, a_2, \ldots, a_N)$ and $B = (b_1, b_2, \ldots, b_N)$ are $N$-bit binary numbers, the Hamming distance $D_H$ of $A$ and $B$ is the sum of different bits and is defined as follows:

$$D_H = \sum_{i=1}^{N} \left( a_i \text{XOR} b_i \right). \tag{1}$$

where "XOR" is the exclusive OR.

Fig. 1 shows the circuit configuration of the proposed Hamming distance detection circuit using a neuron CMOS inverter. Fig. 2 shows the equivalent circuit of Fig. 1.
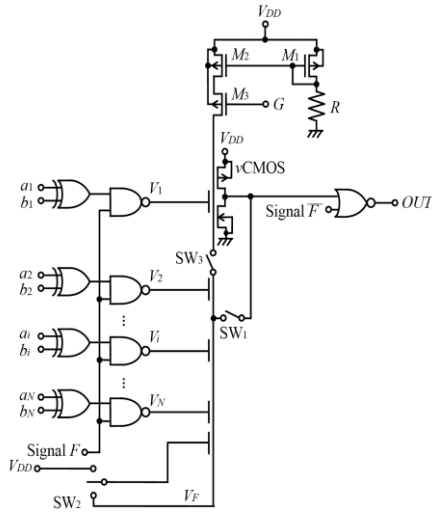

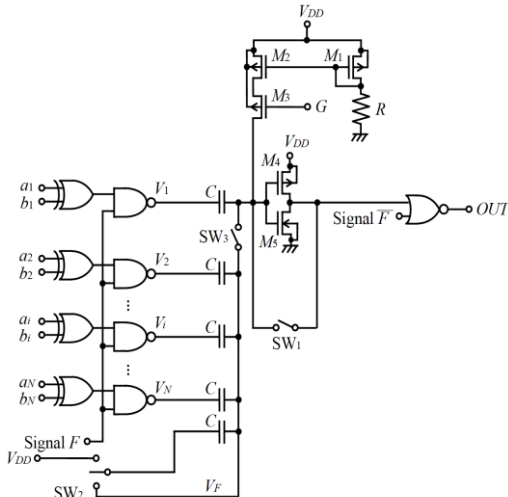
Fig. 1. Circuit configuration of the proposed circuit.



Fig. 2. Circuit configuration of the equivalent circuit of the proposed circuit.

In Fig. 1 and Fig. 2, $V_{DD}$ is the supply voltage, $A = (a_1, a_2, \ldots, a_N)$ is the input data, $B = (b_1, b_2, \ldots, b_N)$ is the reference data, and $F$ and $G$ are the control signal. The neuron CMOS inverter $v$CMOS in Fig. 1 is equivalent to the circuit consisting of an inverter with capacitors $C$ and an inverter with transistors $M_4$ and $M_5$ in Fig. 2, and the input terminal-to-floating gate capacitance $C$ of the $v$CMOS is designed to be all equal.

First, the control signal $F$ is set to a low-level, $G$ is set to a high-level, switch $SW_1$ is turned ON, $SW_2$ is connected to the lower side, and $SW_3$ is turned ON. For this operation, the floating gate voltage $V_F$ of $v$CMOS is equal to the threshold voltage $V_{TH}$, which is expressed by

$$V_F = V_{TH} \tag{2}$$

Since the control signal $F$ is a low-level, the outputs of all NANDs become a high-level and the output OUT becomes a low-level.

Next, after $SW_1$ is turned OFF, $SW_2$ is connected to the upper side. At this point, the change in the floating gate voltage of $v$CMOS, $\Delta V_F$, when the voltage at one of the input terminals of the CMOS changes to $\Delta V$ is expressed as follows:

$$\Delta V_F = \frac{C}{C_T} \Delta V. \tag{3}$$

where $C_T$ in the equation is the sum of the capacitance between the input terminal and the floating gate of $v$CMOS, and is expressed as follows:

$$C_T = (N+1)C. \tag{4}$$

When $SW_2$ is connected to the upper side, the voltage at the bottom input terminal of the $v$CMOS in Fig. 1 changes from $V_{TH}$ to $V_{DD}$, and the floating gate voltage $V_F'$ at this time becomes

$$V_F' = V_{TH} + \frac{C}{C_T} \left( V_{DD} - V_{TH} \right). \tag{5}$$

From this equation, $V_F'$ exceeds the threshold voltage $V_{TH}$, so the output OUT of $v$CMOS becomes a low-level.

When the control signal $F$ is set to a high-level, the output $V_i$ of the NAND changes from a high-level to a low-level if the $i$th bit $a_i$ of the input data and the $i$th bit $b_i$ of the reference data are not equal. If the Hamming distance between the input data $A = (a_1, a_2, \ldots, a_N)$ and the reference data $B = (b_1, b_2, \ldots, b_N)$ is $D_H$, the output of $D_H$ NAND changes from the supply voltage $V_{DD}$ to 0V. When the floating gate voltage $V_F$ is $V_F''$ at this time, it is expressed by the following equation.

$$V_F'' = V_{TH} + \frac{C}{C_T} \left( V_{DD} - V_{TH} \right) - D_H \frac{C}{C_T} V_{DD} \tag{6}$$

From this equation, the floating gate voltage $V_F''$ is below the threshold voltage $V_{TH}$, so the output of $v$CMOS is at a high-level and the output OUT remains at a low-level.

Finally, SW$_3$ is turned off, and the control signal $G$ is set to a low-level. With SW$_3$ turned OFF, the capacitance between the input terminal and the floating gate of the $v$CMOS is disconnected except for the first input terminal from the top. When the control signal $G$ becomes a low-level, MOS transistor M$_3$ turns ON and a constant current begins to flow from the current mirror circuit consisting of $R$, $M_1$, and $M_2$. This causes the floating gate voltage $V_F$ to rise linearly from $V_F''$. When this exceeds the threshold voltage $V_{TH}$, the output of the neuron CMOS inverter becomes a low-level and the output becomes a high-level.

When the constant current flowing through M$_3$ is $I$, the time $T$ from when the control signal $G$ is set to a low-level until the output OUT becomes a high-level is expressed by

$$T = \frac{C\left(V_{TH} - V_F''\right)}{I} .\qquad(7)$$

Substituting (6) into this equation gives

$$T = \frac{C\left\{V_{TH} - V_{TH} - \dfrac{C}{C_T}\left(V_{DD} - V_{TH}\right) + D_H \dfrac{C}{C_T}V_{DD}\right\}}{I}.\qquad(8)$$

By substituting (4) into this and rearranging the equation, the time $T$ can be expressed as follows:

$$T = D_H \frac{C}{I(N+1)}V_{DD} - \frac{C}{I(N+1)}\left(V_{DD} - V_{TH}\right).\qquad(9)$$

The time difference $\Delta T$ when the Hamming distance differs by 1 is expressed by

$$\Delta T = \frac{C}{I(N+1)}V_{DD}\qquad(10)$$

From Eq. (9) and (10), it can be seen that the time $T$ from when the control signal $G$ becomes a low-level until the output OUT becomes a high-level is proportional to the Hamming distance. By measuring this time difference, the proposed Hamming distance detection circuit can detect the Hamming distance between two data. Furthermore, it can be seen that although the detection time increases as the Hamming distance $D_H$ increases, the detection time decreases as the number of data bits in data $N$ increases.

From the above, the proposed circuit reduces the capacitance between the input terminal and the floating gate of the $v$CMOS by controlling SW$_3$, thereby reducing the charging time. Therefore, the proposed circuit does not decrease the detection speed even when the number of data bits $N$ increases and can operate faster than the conventional circuit.

## III. Simulation Results

The proposed Hamming distance detection circuit was simulated in HSPICE, HSPICE, a type of Simulation Program with Integrated Circuit Emphasis (SPICE), for the case where the number of bits is 8. The simulations were performed using SPICE parameters for ROHM's

0.18 μ CMOS process, with a supply voltage of 1.8 V for $V_{DD}$ and a threshold voltage $V_{TH}$ for the floating gate of the neuron CMOS inverter designed to be 0.9 V, half of $V_{DD}$. The equivalent circuit shown in Fig. 2 was used for the simulation.

Fig. 3 shows the simulation results of the floating gate voltage of the neuron CMOS inverter when reference data with a Hamming distance of 1–4 is input. In this figure, $t_1$ represents the point in time when the control signal $F$ is set to a low-level, SW$_1$ is turned ON, SW$_2$ is connected to the lower side, and SW$_3$ is turned ON; $t_2$ represents the point in time when SW$_1$ is turned OFF and SW$_2$ is connected to the upper side; $t_3$ represents the point in time when the control signal $F$ is set to a high-level; $t_4$ represents the time when SW$_3$ is turned OFF and the control signal $G$ is set to a low-level. The floating gate voltage $V_F$ is equal to the threshold voltage $V_{TH}$ at the time $t_1$ and rises and exceeds $V_{TH}$ at $t_2$. At the time $t_3$, the floating gate voltage $V_F$ decreases in proportion to the Hamming distance. Finally, at the time $t_4$, the floating gate voltage begins to increase linearly. When the floating gate voltage exceeds the threshold voltage of the neuron CMOS inverter, its output changes from a high-level to a low-level. The simulation results show that the time it takes for the output to change is proportional to the Hamming distance. The proposed circuit can detect the Hamming distance between the two data by this time difference.
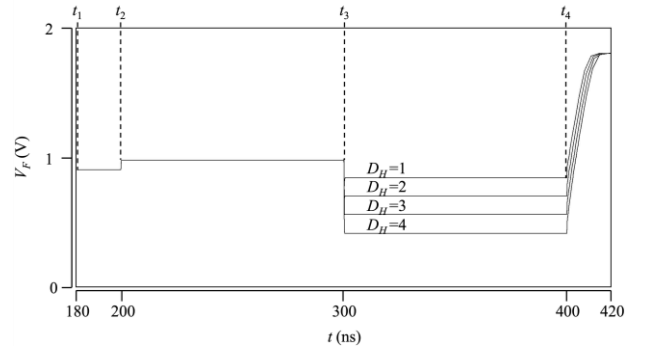


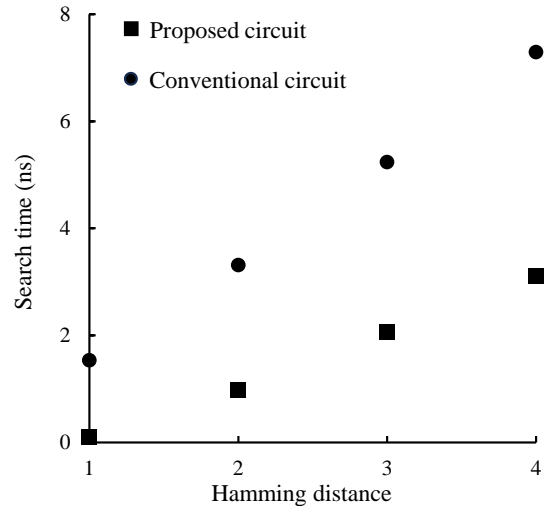Fig. 3. Simulation results of the floating gate voltage.



Fig. 4. Relationship between the search time and Hamming distance.

Fig. 4 summarizes the detection times of the proposed circuit and the conventional circuit in [20]. From this figure, it can be seen that the proposed circuit operates faster than the conventional circuit. In the conventional circuit and the proposed circuit, the sum of the capacitances between the input terminals and the floating gate of the neuron CMOS inverter increases with the number of bits. Therefore, in the conventional circuit, the time until the floating gate voltage reaches the threshold voltage after $G$ is set to a low-level increases in proportion to the number of bits. However, the proposed circuit can achieve high-speed operation even as the number of bits increases by disconnecting the capacitance other than the top one during charging.

## IV. CONCLUSION

In this study, the authors proposed a novel Hamming distance detection circuit using the neuron CMOS inverter. The proposed Hamming distance detection circuit solves the problem of increasing the detection time with increasing the number of bits, which has been a problem in the conventional circuit, by changing the capacitance between the input terminal and the floating gate of the neuron CMOS inverter.

The desired operation of this circuit was confirmed by HSPICE simulation. Furthermore, it was found that the proposed circuit can operate even faster than the conventional circuit.

In future work, it is planned to fabricate a prototype chip of the proposed circuit and conduct experiments and evaluations using the chip.

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